IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 1, Issue 1, March, 2013
ISSN: 2320 - 8791
www.ijreat.org

Processing Element Architecture for Meteorological Application

Jamuna Rani.G[1] and V.J.K. Kishor Sonti[2]

[1,2] ECE Department, Sathyabama University, Chennai, Tamil Nadu 600 017, India.

Abstract

Weather Prediction and warnings are the most essential services provided by meteorological department. Weather forecasts are used to take preventive measure, safeguard the life and property. Super fast computers, meteorological satellites and weather radars are the tools playing a vital role in improving to predict the weather. It delivers timely and authoritative forecasts and early warnings, thereby contributing to reducing the risk of disasters from natural hazards. It focuses on severe weather forecasts and warnings for developing countries to warn the heavy rain, strong winds. The coding for processing element design is done in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language) while the synthesis and simulation is done using Xilinx ISE9.1i.

Keywords: *Matrix Multiplication, Systolic Array, Forecast and Weather prediction.*

1. Introduction

In late 1970's introduction of systolic arrays had an enormous impact on the area of special purpose computing. In 1985, "Systolic array apparatuses for matrix computations" had implemented [1]. In 1996, "2D Matrix multiplication on a 3D systolic array" was implemented. This paper introduces one algorithm for 2D matrix multiplication using 3D systolic array [2]. In 2007, "FPGA Implementation of optimal planar systolic arrays for orthogonal matrix multiplication" was implemented [3]. In 2010, "Matrix Multiplication on Linear Bidirectional Systolic Arrays" was implemented [4]. In 2012, "32-bit N*N matrix multiplication; Performance evaluation for Altera FPGA, i5 Clarkdale, and Atom Pineview-D Intel general purpose processors" were implemented. This paper survey and explore different low power design techniques for FPGA and processors [5].

2. Matrix Multiplication

Matrix computation used in many important applications, such as digital signal, image and video processing, numerical analysis, computer graphics and vision, etc. The nature of matrix multiplication algorithms is perfectly suited to parallel exploitation [3].

Matrix multiplication plays a central role in numerical linear algebra, since one has to compute this product in several stages of almost all numerical algorithms, as well as in many technical problems, especially in the area of digital signal processing, pattern recognition, plasma physics, weather prediction, etc. Therefore, finding an efficient algorithm for performing these computations is at the focus of interest of many researchers. Matrix multiplication is a very regular computation and lends itself well to parallel implementation [4]. To handle matrix multiplication, 2D and 1D systolic array have been proposed.

3. Systolic Architecture

Figure1. Shows structure of the Systolic Architecture.

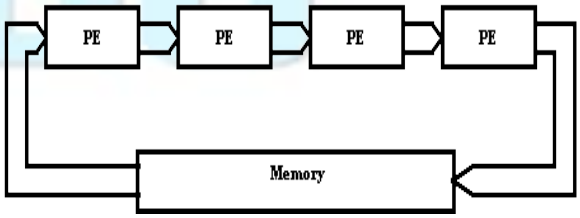

Figure 1. Systolic Architecture

Systolic networks are class of pipelined array architectures which rhythmically compute and pass data through the processing element. A Systolic

Array (SA) features the important properties of modularity, regularity, local interconnection, a high degree of pipelining and high synchronized multiprocessing.

By using systolic processing, computational-intensive tasks, including matrix multiplication can often be accomplished in a relatively simple and inexpensive manner, without increasing I/O requirements. The major features of adopting a SA for special-purpose processing architectures are: simple and regular design, concurrency, nearest-neighbor communication and balancing computations with the I/O.

A Systolic array system of processor is provided in the form of a mesh connected network which rhythmically computes and passes data through the system. Each processor in the system regularly feeds data in and out, each time performing some computation, so that a regular flow of data is kept up in the network. In these arrays, data pass through many cells, and are used by different cells for computation, before being returned to the memory. As the same data are used repeatedly for many computations, the computational throughput is increased without a need for increasing the I/O bandwidth or using a local memory. Furthermore, since the cells of the systolic arrays are simple and regular, they are easier and cheaper to design. [2]

4.Processing Element Architecture Design

Figure 2. Shows the RAM Architecture retains the value of temperature, humidity and wind velocity for 365 days which generates the outputs as temperature data out, humidity data out and wind velocity data out. For this project past six years of temperature, humidity and wind velocity are written into the RAM. For example from 2007 to 2012, data's are stored and leap years 366 data's are written into the memory (leap years 2008 and 2012). These data's are stored in matrix form whose address lines are days (row) and temperature, humidity and wind velocity are data lines (column).

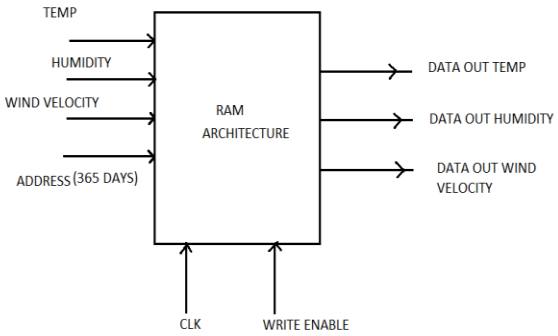

Figure 2. RAM Architecture

Figure 3. Shows constructing processing elements. For this project six processing elements are required, each processing element has inputs (temperature, humidity and wind velocity) from RAM architecture and reference value of temperature, reference value of humidity and reference value of wind velocity respectively.

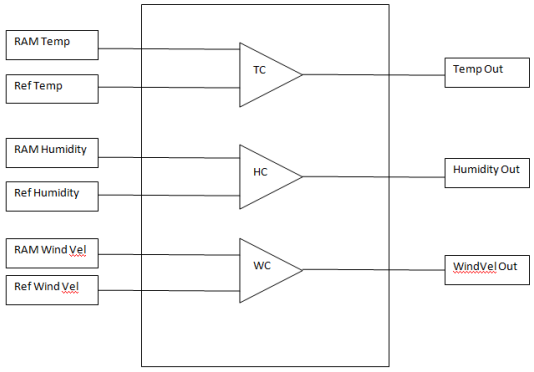

Figure 3.Processing Element

Each processing element has three comparators to compare temperature value, humidity value and wind velocity value. An output of comparator generates the value in binary form.

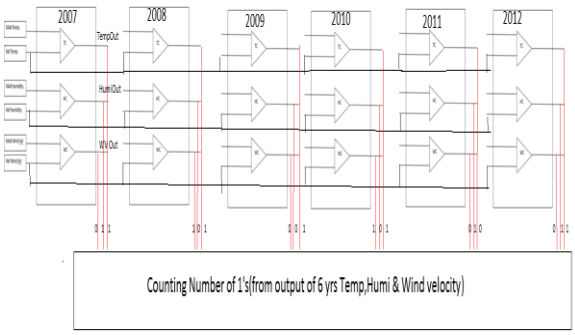

Figure 4.Constructing Processing Element for six years

Enable to compare the value of temperature, humidity and wind velocity with the reference value of temperature, humidity and wind velocity using suitable comparator and it indicates either 1 or 0 based on greater or lesser value.

Figure 4. Shows the processing element architecture design for meteorological application. An output of comparator is in the form of binary.

5. Simulation Results

Processing Element design for metrological application is implemented using VHDL.VHDL code using ModelSim SE 5.5 simulator. The entire code is completely synthesized. The synthesis is done using Xilinx Synthesis Tool (XST) available with Xilinx ISE 9.1i.The simulation and the output waveform for metrological application using Systolic Architecture as follows.

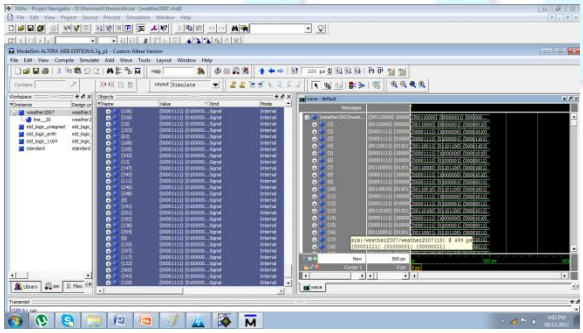

Figure 5. Simulation result for weather data of one year.

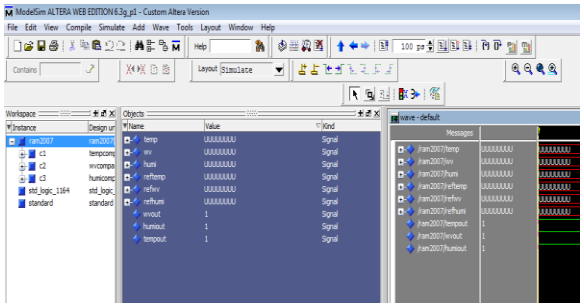

Figure 6. Simulation result for connecting three comparators.

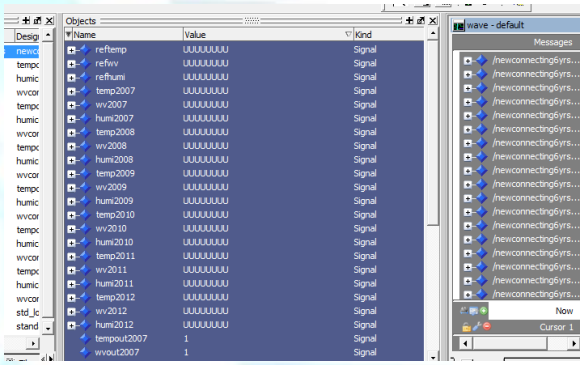

Figure 7 .Simulation result for connecting all the PEs

6. Conclusion

Weather affects every aspect of lives, either directly or indirectly. The ability to forecast the weather accurately is a major part of economy and society. Weather forecasting is enormously sophisticated and expensive, involving the use of satellite technology, supercomputers and phenomenally large streams of data which are continuously being updated. Prediction allows reducing impact and thus saving money.

On the other way it makes full use of the advantages of modern VLSI, which are high integration, low cost and easy to achieve the operation of parallel computing. Therefore, it improves the speed of solving super-high dimensional group greatly.

7. References

[1] Kung et al. ,*Systolic array apparatues for matrix multiplications*, United States patent-1985.

[2] Slim lakhani, Yi Wang, Aleksander Milenkovic and Veljko Milutinovic,*2D matrix multiplication on a 3D systolic array*,Microelectronic Journal27(1996).

[3] I.N. Tselepis, M.P.Bekakos, I.Z. Milovanovic and E.I.Milovanovic, *FPGA Implentation of Optimal planar Systolic Arrays for Orthogonal Matrix Multiplication*,March 25-29, 2007 – TUNISIA – 1.

[4] E. I. Milovanovic´, B. M. Randjelovic´, I. Z˘ . Milovanovic´, M. K. Stojc˘ev, *Matrix Multiplication on Linear Bidirectional Systolic Arrays*, SER. A: APPL. MATH. INFORM. AND MECH. vol. 2, 1 11-2010

[5] Izzeldin Ibrahim Mohd, Chay Chin Fatt, and Muhammad N.Marsono,*32-Bit N*N Matrix Multiplication : Performance Evaluation for Altea FPGA, i5 Clarkdale , and atom Pinview-D Intel General purpose Processor*, International Journel of Computer Applications(0975-8887),August 2012.

[6] Kung H.T., Why Systolic Architectures?, *IEEE, Computer*, Vol. 15, No 1, pp. 37-46, Jan 1982.

[7] Kung S.Y., *VLSI Array Processors*, Prentice Hall, Englewood Cliffs, New Jersey, 1988.